



PDP-1449 (Based on Form PTO-1449)

PATENT AND TRADEMARK OFFICE  
INFORMATION DISCLOSURE CITATION

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Sheet 1 of 1

ATTORNEY DOCKET NO.

MP0039.C1

SERIAL NO.

10/786,010

APPLICANT

Pierte Roo

FILING DATE

2/26/2004

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2618

## U.S. PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date
1.	<i>g</i>	6,606,489 B2	8/2003	Razavi et al	—	
2.	<i>g</i>	6,870,881	3/2005	He, Runsheng	—	

## FOREIGN PATENT DOCUMENTS

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1.							

## OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

Ref. Desig.	Examiner's Initials	
1.	<i>A</i>	Stonick et al; "An Adaptive PAM-4 5-Gb/s Backplane Transceiver in 0.25-um CMOS; IEEE Journal of Solid-State Circuits, Vol. 38, No. 3, March 2003; pp. 436-443

Examiner:

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1.	9	6,975,674	12/2005	Phanse et al.	375/219	

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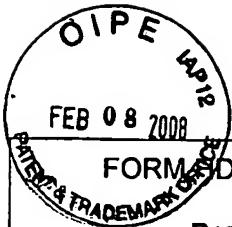
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**U.S. PATENT DOCUMENTS**

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3.	9	6,606,489 B2	08/2003	Razavi et al.	—	
4.	9	6,744,931	06/2004	Komiya et al.	—	
5.	9	6,870,881	03/2005	He, Runsheng	—	
6.	9	6,975,674	12/2005	Phanse et al.	375/219	

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2.	9	Chien et al; "TP 12.4: A 900-MHz Local Oscillator using a DLL-based Frequency Multiplier Technique for PCS Applications"; Journal of IEEE Solid State Circuits; Feb. 2000; pgs. 202-203 and 458
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4.	9	Chien; "Monolithic CMOS Frequency Synthesizer for Cellular Applications"; Solid State Circuits, IEEE Journal of, Vol. 35, Issue 12, Dec. 2000
5.	9	Dally et al; "Digital Systems Engineering"; Cambridge Univ. Press; June 1998; cover and pgs. 390-391

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7.	el	Dehng et al; "A Fast-Lock Mixed-Mode DLL Using a 2-b SAR Algorithm"; IEEE Journal of Solid State Circuits, Vol. 36, No. 10; Oct. 2001; pp. 1464-1471
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50.	<i>Y</i>	Stonick et al; "An Adaptive PAM-4 5-Gb/s Backplane Transceiver in 0.25-um CMOS; IEEE Journal of Solid State Circuits, Vol. 38, No. 3, March 2003; pp. 436-443.

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